CLAIMS

What is claimed is:

1. A method of forming a memory cell, comprising:

forming at least one bottom electrode on a substrate; and

disposing phase change material on the substrate beside the at least one bottom electrode such that the phase change material makes operative contact with the at least one bottom electrode.

2. The method as set forth in Claim 1, further comprising providing a conducting element at least partially disposed within the substrate wherein the conducting element makes operative contact with the at least one bottom electrode.

3. The method as set forth in Claim 2, wherein the forming of at least one bottom electrode comprises:

forming a pad layer on the substrate, the pad layer having sidewalls substantially parallel to a length dimension of the pad layer; and

forming at least one bottom electrode on at least one of the sidewalls.

4. The method as set forth in Claim 3, wherein the forming of a pad layer comprises:

disposing a layer of first material on the substrate; and

etching the layer of first material to expose at least part of the conducting element and to form the pad layer.

5. The method as set forth in Claim 4, wherein the disposing of a layer of first material comprises disposing a layer formed substantially of dielectric material.

6. The method as set forth in Claim 3, wherein the forming of at least one bottom electrode on at least one of the sidewalls comprises:

disposing a layer of conducting material over the pad layer, at least one of the sidewalls of the pad layer, and the substrate; and

etching back the layer of conducting material to leave conducting material on at least one of the sidewalls of the pad layer to thereby form the at least one bottom electrode, the at least one bottom electrode having a length dimension substantially parallel to the length dimension of the pad layer.

7. The method as set forth in Claim 3, wherein the disposing of phase change material comprises:

forming a layer of insulating material over the pad layer, the at least one bottom electrode, and the substrate;

forming a trench in the insulating material extending through the pad layer and the at least one bottom electrode to the surface of the substrate, the trench being oriented substantially at a right angle to the length dimension of the at least one bottom electrode, wherein the forming of the trench removes a section of the at least one bottom electrode thereby exposing a plane end surface of the at least one bottom electrode; and

disposing a layer of phase change material over the insulating material, whereby the phase change material fills the trench and enables the phase change material to make contact with the exposed plane end surface of the at least one bottom electrode.

8. The method as set forth in Claim 7, wherein the forming of a layer of insulating material over the pad layer is preceded by removing a portion of the at least one bottom electrode and the pad layer, thereby forming a gap that exposes the surface of the substrate in a direction transverse to the length dimension of the pad layer.

9. The method as set forth in Claim 6, further comprising:

disposing a layer of conducting material over the phase change material; and

etching the conducting material and phase change material to form a top electrode operatively connected with the phase change material.

10. The method of Claim 1, wherein the disposing of a phase change material comprises disposing chalcogenide material.

11. A semiconductor element produced by the method of Claim 1.

12. A semiconductor element produced by the method of Claim 6.

13. A semiconductor element produced by the method of Claim 7.

14. A semiconductor element produced by the method of Claim 10.

15. A memory cell, comprising:

a conducting element at least partially disposed within a substrate;

a bottom electrode at least partially disposed on a surface of the substrate and operatively coupled with the conducting element; and

phase change material at least partially disposed on the surface of the substrate and operatively coupled with the bottom electrode.

16. The memory cell as set forth in Claim 15, wherein:

the bottom electrode has dimensions of length, height, and width;

the bottom electrode has its length substantially parallel to the substrate;

the bottom electrode includes a plane end surface formed substantially at a right angle to the length; and

the plane end surface forms an operative contact with the phase change material.

17. The memory cell as set forth in Claim 15, further comprising a pad layer disposed on the surface of the substrate wherein the bottom electrode is formed on a sidewall of the pad layer.

18. The memory cell as set forth in Claim 17, wherein:

the pad layer comprises a top surface, a bottom surface, and at least two sidewalls disposed between the top and bottom surfaces; and

the bottom electrode is formed on one of the at least two sidewalls.

19. The memory cell as set forth in Claim 18, the conducting element comprising a first conducting element, the bottom electrode comprising a first bottom electrode, and the memory cell further comprising:

a second conducting element at least partially disposed within the substrate; and

a second bottom electrode formed on another one of the at least two sidewalls of the pad, the second bottom electrode being operatively coupled with the second conducting element, wherein the phase change material is operatively coupled with the second bottom electrode.

20. The memory cell as set forth in Claim 19, wherein the first and second conducting elements are formed of tungsten.

21. The memory cell as set forth in Claim 19, wherein the pad layer is disposed between the first bottom electrode and the second bottom electrode.

22. The memory cell as set forth in Claim 15, further comprising a top electrode disposed on the phase change material.

23. The memory cell as set forth in Claim 15, wherein the phase change material comprises chalcogenide material.

24. An array of memory cells formed at least partially in a substrate, the array being organized into rows and columns with memory cells at intersection of rows and columns, each memory cell in the array comprising a transistor having a source, a drain, and a gate, the gates of transistors in each column being operatively connected with a common word line, and the drains of transistors in each row being operatively connected with a common bit line, each memory cell comprising:

a conducting element at least partially disposed within the substrate, the conducting element being operatively connected with the source of a corresponding transistor;

a pad layer disposed on the substrate;

a bottom electrode formed on a sidewall of the pad layer, the bottom electrode being operatively coupled with the conducting element;

phase change material at least partially disposed on the substrate and operatively coupled with the bottom electrode; and

a top electrode formed of conducting material disposed on the phase change material and establishing operative contact with the phase change material.

25. The array of memory cells as set forth in Claim 24, wherein the phase change material comprises chalcogenide material.